COE 202, Term 052

Fundamentals of Computer Engineering

HW# 5

Q.1. Design a combinational circuit that detects an error in the representation of a decimal digit in BCD. In other words, obtain a logic diagram whose output is equal to 1 when the inputs contain any one of the six unused bit combinations in the BCD code.

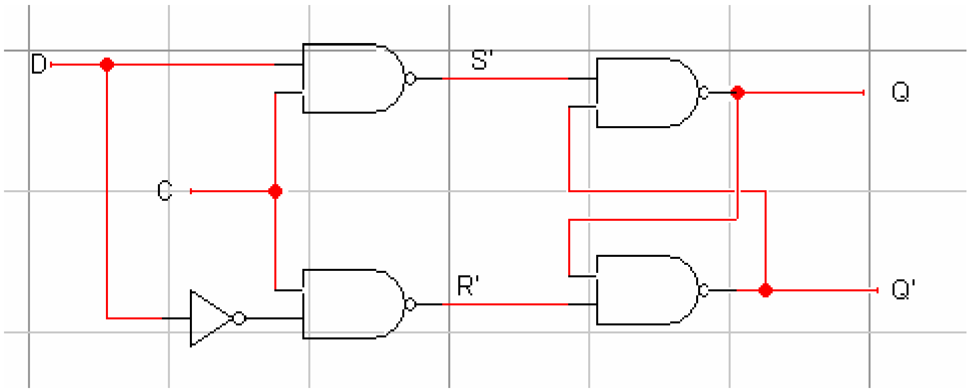
Q.2. Implement a full-adder using a dual 4x1 multiplexer.

Q.3. It is required to design a 4-bit ripple-borrow subtractor to find the subtraction X-Y for the two unsigned numbers, $X=X_3-X_0$, and $Y=Y_3-Y_0$. Design a 1-bit full subtractor and show how it can be used to construct the 4-bit subtractor.

Q.4. Design two simplified combinational circuits that generate the 9's complement of (a) a BCD digit and (b) an excess-3 digit. Then compare the gate and literal count of the two circuits. Assume in both cases that input combinations not corresponding to decimal digits give don't care outputs.

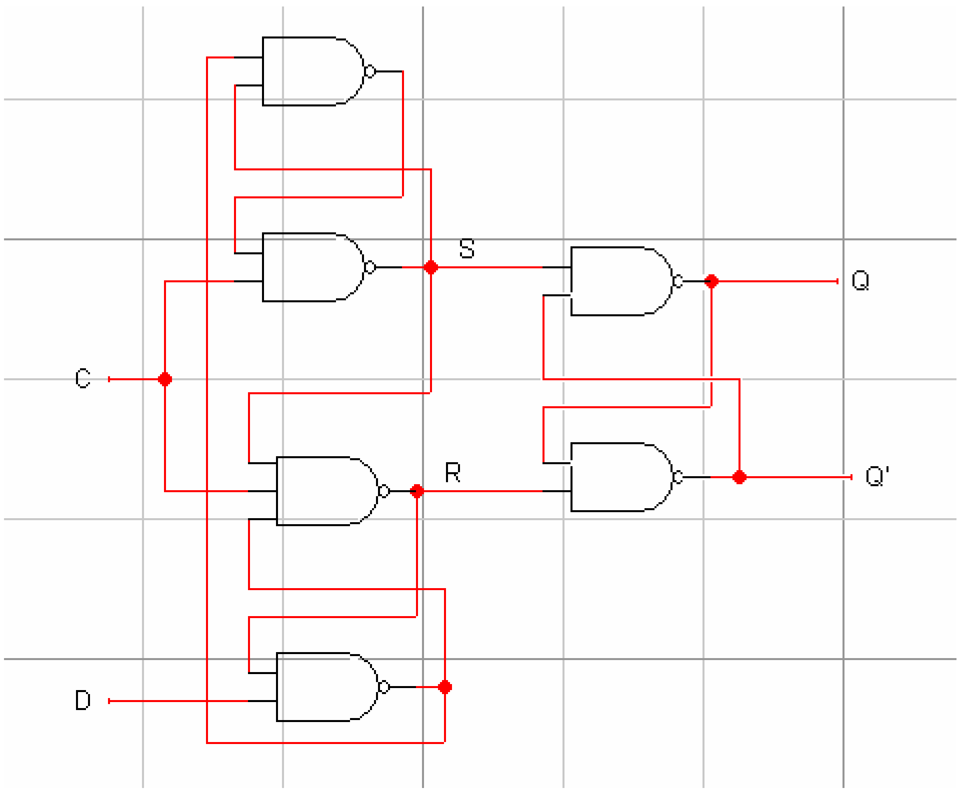
Q.5. Construct a BDC adder-subtractor using a BCD adder and the 9's complement designed in Q3, as well as other logic or functional blocks as necessary. Use block diagrams for the components, showing only inputs and outputs where possible.

Q.6. The D-latch shown below can be constructed with only four NAND gates. This can be done by removing the inverter and connecting the output of the upper NAND gate (connected to the D input) to the input of the lower NAND gate (Connected to D'). Use manual or computer-based logic simulation to verify that the new circuit is functionally the same as the original one.



Q.7. Obtain the logic diagram of the D-latch give in Q6, using NOR gates only.

Q.8. A popular alternative design for positive-edge-triggered D flip-flop is shown below. Simulate the circuit to determine that its functional behavior is identical to that of a D flip-flop.



Q.9. Show the design of the following flip-flops using SR latches and external gates:

(i) A negative-edge triggered D-FF.

(ii) A negative edge-triggered JK-FF.

(iii) A positive-edge triggered T-FF.

Q.10. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

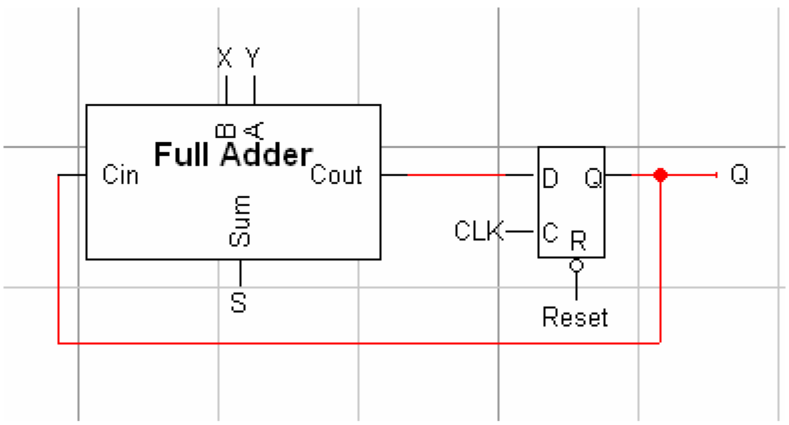
$D_A = X` Y + X A$ $D_B = X` B + X A$ $Z = B$

(i) Draw the logic diagram of the circuit.

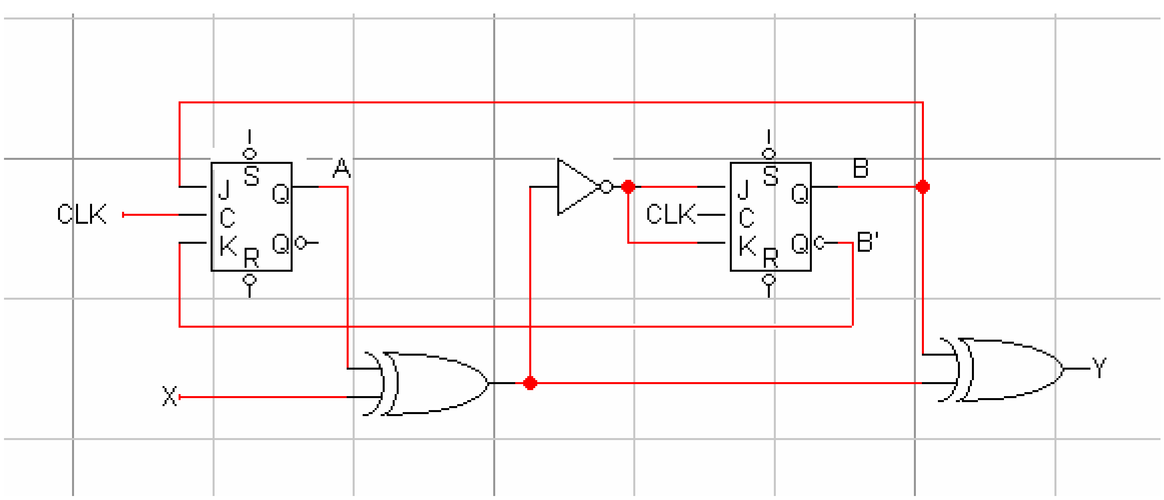
(ii) Derive the state table.

(iii) Derive the state diagram.

Q.11. A sequential circuit has one flip-flip Q, two inputs X and Y, and one output S. The circuit consists of a full adder circuit connected to a D flip-flop, as shown below. Derive the state table and state diagram of the sequential circuit.



Q.12. A sequential circuit has two JK flip-flops, one input X, and one output Y. The logic diagram of the circuit is shown below. Derive the state table and state diagram of the circuit.

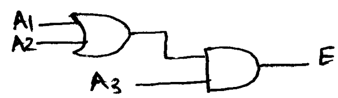


HW#5

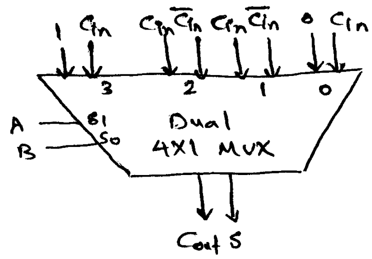
Q1 The output is 1 if the BCD code is in the range 1010 – 1111.

A_3A_2 \ A_1A_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

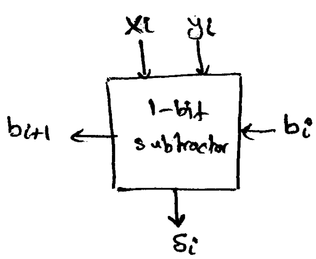
$$E = A_3A_2 + A_3A_1$$
$$= A_3(A_2 + A_1)$$



Q2 Full adder



Q3



b_i	x_i	y_i	b_{i+1}	s_i
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

b_i \ $x_i y_i$	00	01	11	10
0	0	1	0	0
1	1	1	1	0

$$b_{i+1} = \bar{x}_i y_i + b_i \bar{x}_i + b_i y_i$$

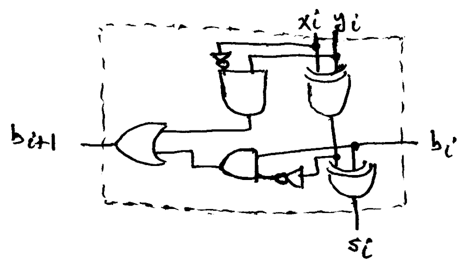
$$= \bar{x}_i y_i + b_i (y_i + \bar{x}_i)$$

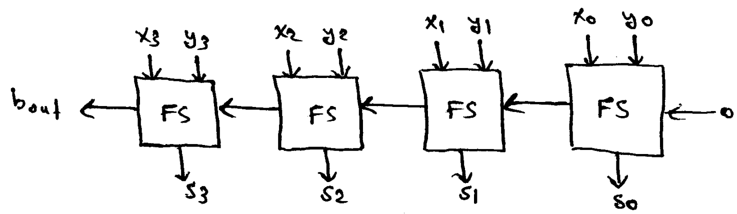
$$= \bar{x}_i y_i + b_i (y_i \oplus \bar{x}_i)$$

$$= \bar{x}_i y_i + b_i (y_i \oplus x_i)'$$

b_i \ $x_i y_i$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$s_i = x_i \oplus y_i \oplus b_i$$





Q4 9's complement

(a) BCD digit

Digit	x_3	x_2	x_1	x_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	0
2	0	0	1	0	0	1	1	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	0	0
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	0	1	0
8	1	0	0	0	0	0	0	1
9	1	0	0	0	0	0	0	0

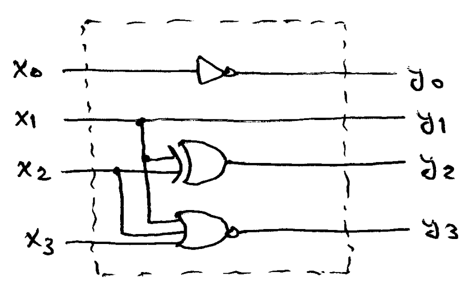
$y_0 = \overline{x_0}$, $y_1 = x_1$

x_3x_2 \ x_1x_0	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	x	x	x	x
10	0	0	x	x

$$y_2 = x_2\overline{x_1} + \overline{x_2}x_1$$
$$= x_2 \oplus x_1$$

x_3x_2 \ x_1x_0	00	01	11	10
00	1	1	0	0
01	0	0	0	0
11	x	x	x	x
10	0	0	x	x

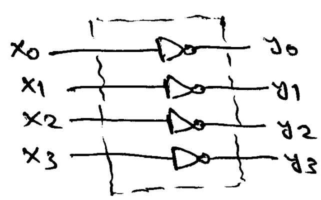
$$y_3 = \overline{x_3}\,\overline{x_2}\,\overline{x_1}$$



(b) Excess-3 digit

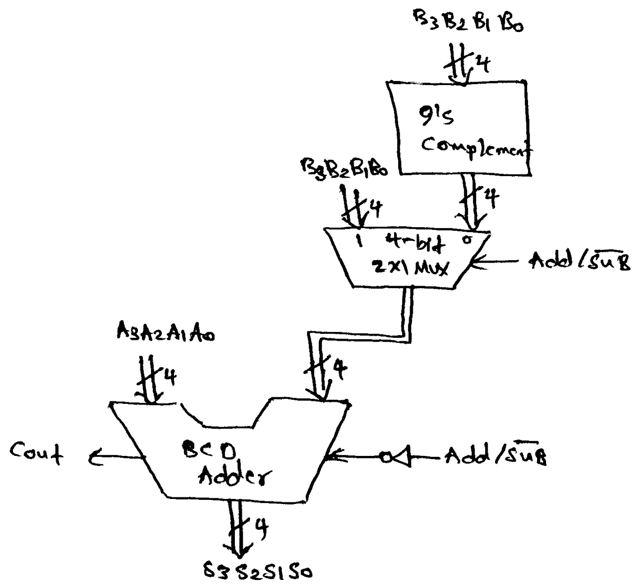
Digit	x_3	x_2	x_1	x_0	y_3	y_2	y_1	y_0
0	0	0	1	1	1	1	0	0
1	0	1	0	0	1	0	1	1
2	0	1	0	1	1	0	1	0
3	0	1	1	0	1	0	0	1
4	0	1	1	1	1	0	0	0
5	1	0	0	0	0	1	1	1
6	1	0	0	1	0	1	1	0
7	1	0	1	0	0	1	0	1
8	1	0	1	1	0	1	0	0
9	1	1	0	0	0	0	1	1

$y_0 = \overline{x_0}$, $y_1 = \overline{x_1}$, $y_2 = \overline{x_2}$, $y_3 = \overline{x_3}$

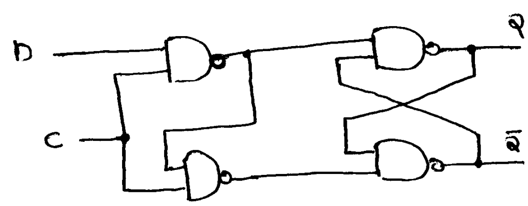


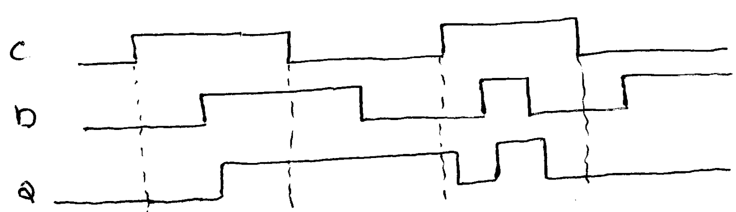
(c) we can see that for the excess-3 code, the 9's complement circuit has 4 literals and 4 inverter gates. However, for the BCD code, the 9's complement circuit has 9 literal and one inverter, one NOR, and one XOR gate. This is the advantage of using the excess-3 code as the 9's complement is obtained by finding the 1's complement of the code.

Q5 BCD Adder - Subtractor

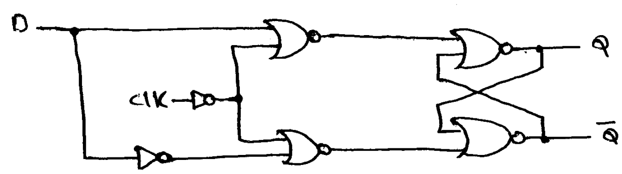


Q6 Modified D-latch

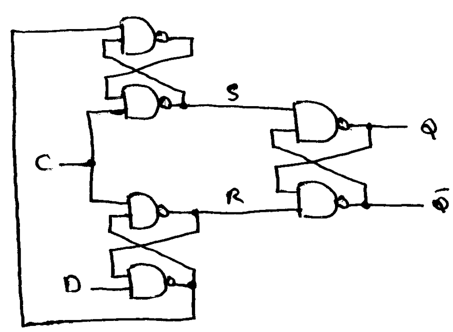


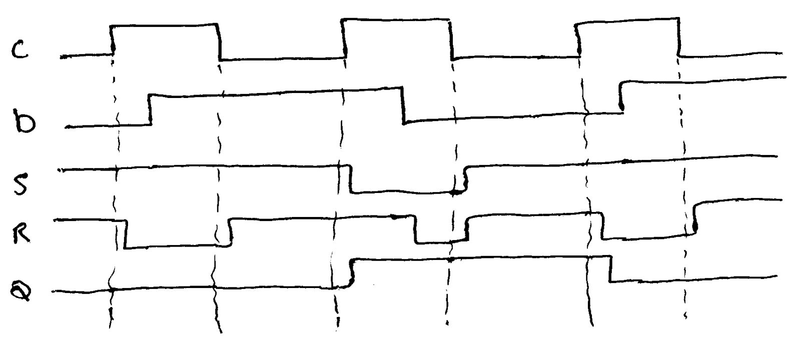


Q7 D latch with NOR gates only



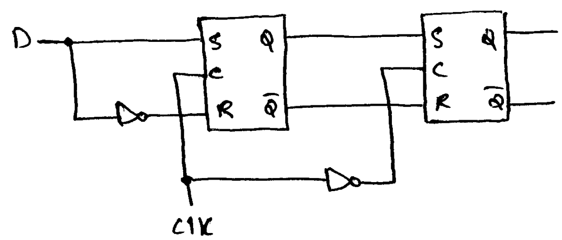
Q8 Alternative positive-edge-triggered D flip-flop



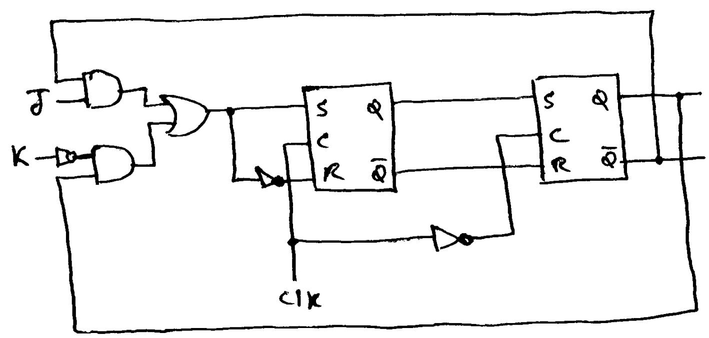


Q9

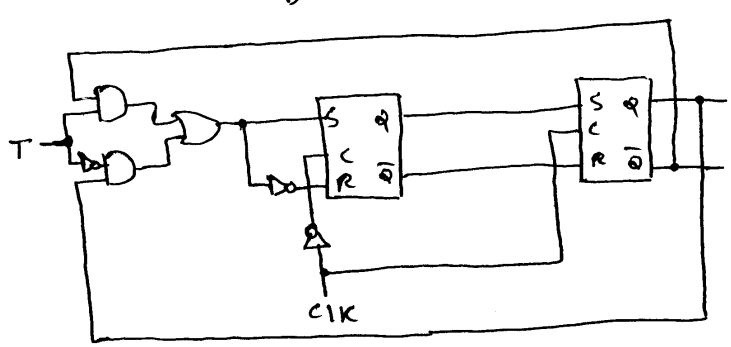
(i) Negative-edge triggered D-FF



(ii) Negative-edge triggered JK-FF



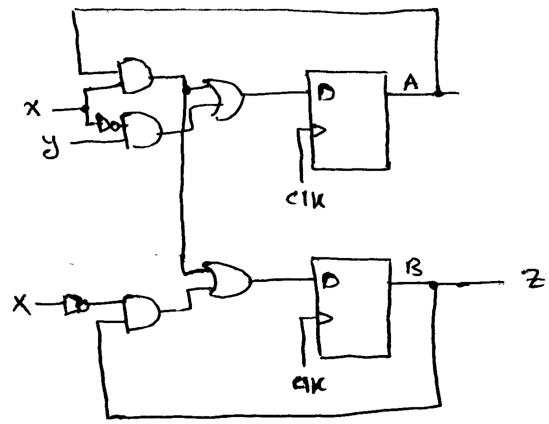
(iii) Positive-edge triggered T-FF



Q10

$$D_A = \bar{X}Y + XA \quad , \quad D_B = \bar{X}B + XA \quad , \quad Z = B$$

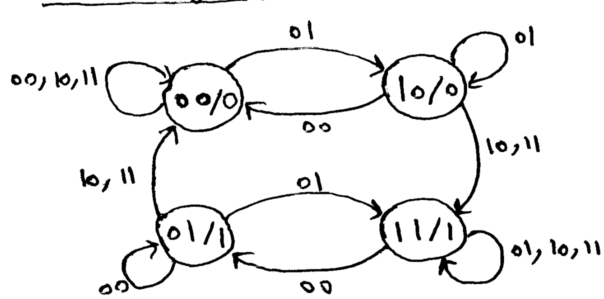
(a)



(b) State Table:

Current State AB	Next State xy=00 AB	xy=01 AB	xy=10 AB	xy=11 AB	output Z
0 0	0 0	1 0	0 0	0 0	0
0 1	0 1	1 1	0 0	0 0	1
1 0	0 0	1 0	1 1	1 1	0
1 1	0 1	1 1	1 1	1 1	1

(c) State Diagram:



* Note that this circuit has a Moore model.

* Note that this circuit has several synchronizing sequences. For example, {00, 11} synchronizes it to state 00.

Q11

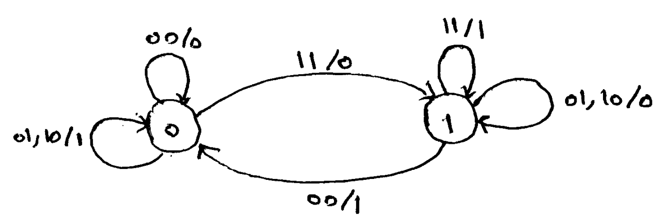
$$D_z = xy + xz + yz$$

$$S = x \oplus y \oplus z$$

State Table:

Current state z	Inputs x	Inputs y	Next state z	Output S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

State Diagram:



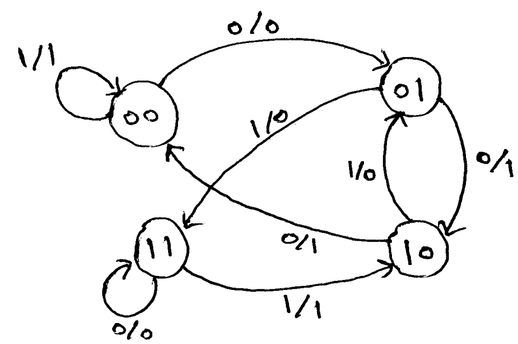
This circuit is a mealy model.

Note that this circuit has synchronizing sequence. For example, {00} synchronizes the circuit to state 0. Also, {11} synchronizes it to the 1 state.

Q12 $J_A = B$, $K_A = \overline{B}$, $J_B = (A \oplus X)'$, $K_B = (A \oplus X)'$, $Y = A \oplus B \oplus X$

Current State		Input	Next State		FFs Inputs				output
A	B	X	A	B	J_A	K_A	J_B	K_B	Y
0	0	0	0	1	0	1	1	1	0
0	0	1	0	0	0	1	0	0	1
0	1	0	1	0	1	0	1	1	1
0	1	1	1	1	1	0	0	0	0
1	0	0	0	0	0	1	0	0	1
1	0	1	0	1	0	1	1	1	0
1	1	0	1	1	1	0	0	0	0
1	1	1	1	0	1	0	1	1	1

State Diagram:



This circuit is a mealy model.

Notice that this circuit has no synchronizing sequence.