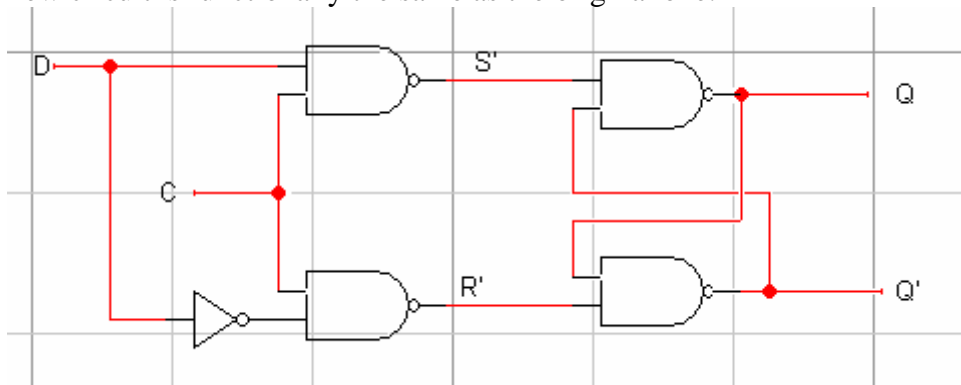
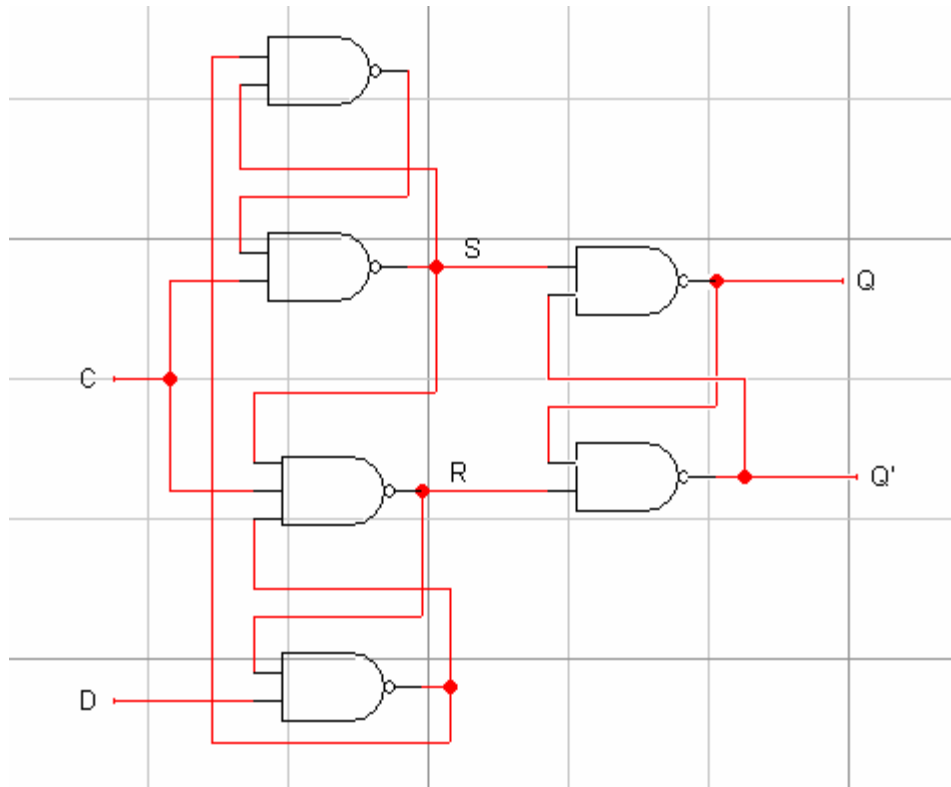


**COE 202, Term 052**  
**Fundamentals of Computer Engineering**  
**HW# 5**

- Q.1.** Design a combinational circuit that detects an error in the representation of a decimal digit in BCD. In other words, obtain a logic diagram whose output is equal to 1 when the inputs contain any one of the six unused bit combinations in the BCD code.
- Q.2.** Implement a full-adder using a dual 4x1 multiplexer.
- Q.3.** It is required to design a 4-bit ripple-borrow subtractor to find the subtraction  $X - Y$  for the two unsigned numbers,  $X = X_3 - X_0$ , and  $Y = Y_3 - Y_0$ . Design a 1-bit full subtractor and show how it can be used to construct the 4-bit subtractor.
- Q.4.** Design two simplified combinational circuits that generate the 9's complement of (a) a BCD digit and (b) an excess-3 digit. Then compare the gate and literal count of the two circuits. Assume in both cases that input combinations not corresponding to decimal digits give don't care outputs.
- Q.5.** Construct a BDC adder-subtractor using a BCD adder and the 9's complement designed in Q3, as well as other logic or functional blocks as necessary. Use block diagrams for the components, showing only inputs and outputs where possible.
- Q.6.** The D-latch shown below can be constructed with only four NAND gates. This can be done by removing the inverter and connecting the output of the upper NAND gate (connected to the D input) to the input of the lower NAND gate (Connected to D'). Use manual or computer-based logic simulation to verify that the new circuit is functionally the same as the original one.



- Q.7.** Obtain the logic diagram of the D-latch give in Q6, using NOR gates only.
- Q.8.** A popular alternative design for positive-edge-triggered D flip-flop is shown below. Simulate the circuit to determine that its functional behavior is identical to that of a D flip-flop.

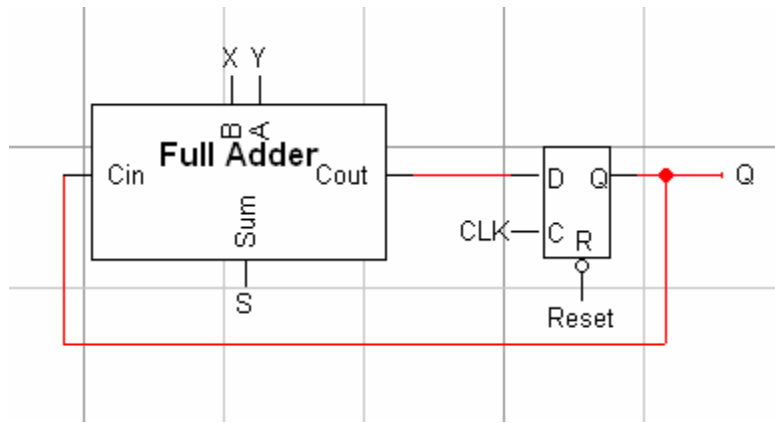


- Q.9.** Show the design of the following flip-flops using SR latches and external gates:
- A negative-edge triggered D-FF.
  - A negative edge-triggered JK-FF.
  - A positive-edge triggered T-FF.

- Q.10.** A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$$D_A = X' Y + X A \qquad D_B = X' B + X A \qquad Z = B$$

- Draw the logic diagram of the circuit.
  - Derive the state table.
  - Derive the state diagram.
- Q.11.** A sequential circuit has one flip-flop Q, two inputs X and Y, and one output S. The circuit consists of a full adder circuit connected to a D flip-flop, as shown below. Derive the state table and state diagram of the sequential circuit.



**Q.12.** A sequential circuit has two JK flip-flops, one input X, and one output Y. The logic diagram of the circuit is shown below. Derive the state table and state diagram of the circuit.

