May 30, 2006

COMPUTER ENGINEERING DEPARTMENT

COE 202

FUNDAMENTALS OF COMPUTER ENGINEERING

Final Exam

Second Semester (052)

Time: 7:30-10:30 AM

Student Name : _____

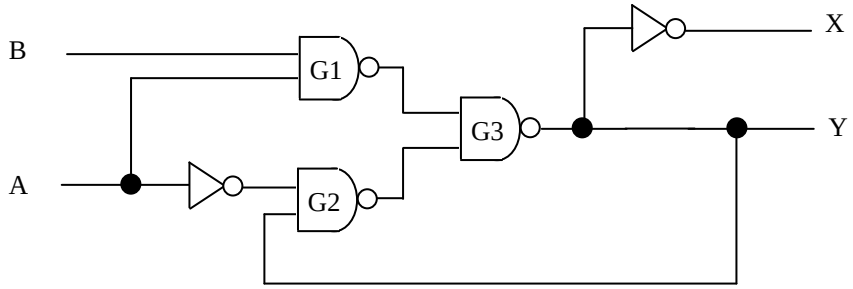
Student ID. : _____

Question	Max Points	Score
Q1	20	
Q2	20	
Q3	15	
Q4	10	
Q5	10	
Q6	10	
Q7	15	
Total	100	

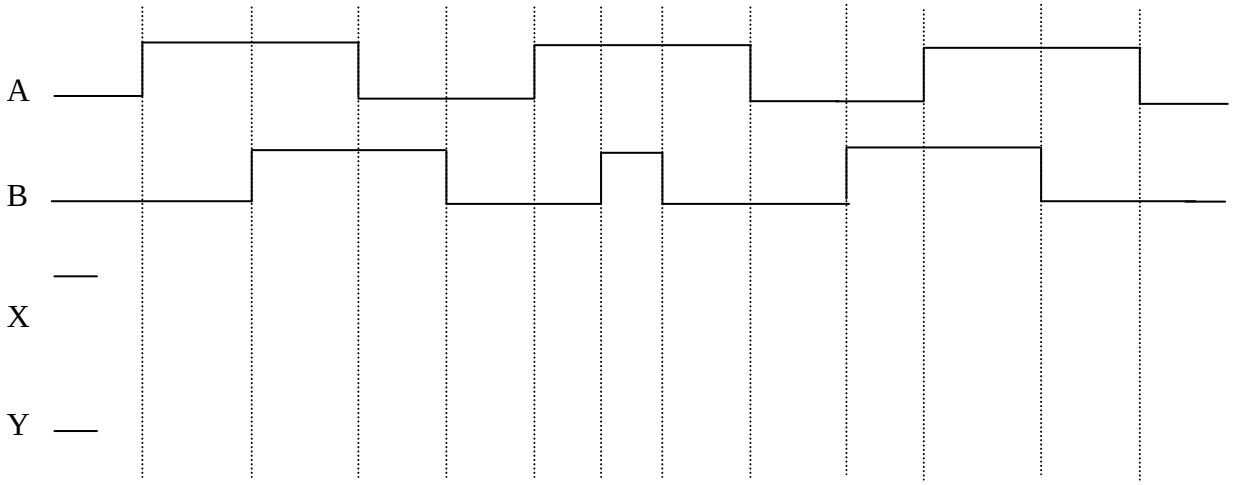
Dr. Aiman El-Maleh

[20 Points]

(Q1) Consider the circuit shown below that has two inputs A, B, and two outputs X , Y:



(i) Draw the timing diagram for the outputs X and Y given the waveforms for the inputs A and B shown below. Assume that Y is initially having the value 0.



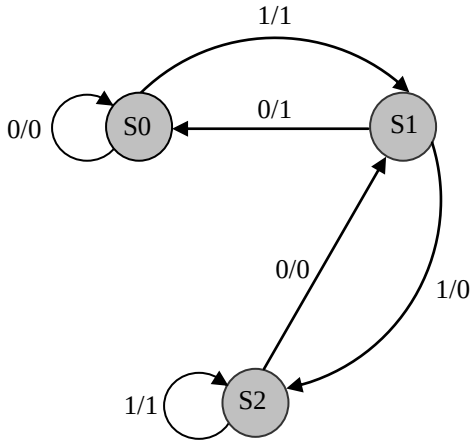
(ii) Does this circuit implement a latch or a flip-flop, and what type? Justify your answer. Indicate what A, B, X, and Y represent.

(**iii**) Show the design of a **positive-edge-triggered T flip-flop** using SR latches.

(iv) Show the design of a **positive-edge-triggered JK flip-flop** using a positive-edge-triggered T flip-flop.

[20 Points]

(Q2) It is required to design a sequential circuit that receives a serial input X, and produces a serial output Z, equivalent to 3*X, i.e., Z=3*X. The state diagram for this circuit is shown below:



Implement the sequential circuit using JK-FFs and the smallest number of gates possible assuming the state assignment: S0=00, S1=01, and S2=10. Show the state table and minimize your equations using K-map method.

[15 Points]

(Q3) A sequential circuit has two D flip-flops A and B, two inputs X and Y, and one output Z. The flip-flop input equations and output function are as follows:

$D_A = B\,X + A\,Y`$
$D_B = A`\,X + B`\,Y$
$Z = X\,A\,B$

(i) Show the implementation of this circuit using a ROM and D-FFs. Determine the size of the ROM that will be used and show the ROM table.

(ii) Obtain the state diagram for this circuit.

[10 Points]

(Q4) Implement the following two functions with a PLA:

$F_1(A, B, C, D)=\Sigma\, m(1, 2, 3, 5, 6, 7, 10, 11, 14, 15)$
$F_2(A, B, C, D)=\Sigma\, m(0, 1, 4, 5, 9, 10, 13, 14)$

Minimize the number of product terms used in the PLA. Show the internal logic of the PLA that will be used to implement these two functions.

[10 Points]

(Q5) A single-input, single-output sequential circuit is to be designed that recognizes the input sequence 01101 applied to its input any time it occurs in the input stream starting from a reset state. If the sequence is detected the output will be 1, otherwise it will be 0. Show the state diagram for this circuit assuming detection of **overlapping** sequences assuming a **Mealy model**. As an example, the input stream 01101101101 will produce the output stream 00001001001.

[10 Points]

(Q6) It is required to design a sequential circuit that has one serial input stream X and produces a serial output stream computing the **2's complement** of X. Obtain the state diagram for this circuit assuming a **Moore model.**

[15 Points]

(Q7) It is required to design a **synchronous 3-bit up-down counter** using positive-edge-triggered D-FFs. The counter has two inputs E and M. If E=0, the counter remains in the same state, regardless of the value of M. When E=1 and M=1, the counter counts up, and when E=1 and M=0, the counter counts down. Show the logic required to make the counter have **Synchronous Reset, RESET**. When RESET=1, the counter is reset to 0.