

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 200 Fundamentals of Computer Engineering
Term 993 Lectures

	Date	Topics	Ref.	Lab
1	U 11/6	Syllabus. Introduction. Digital systems, Introduction to Computer Organization.	1.1	
2	M 12/6	Number systems: Binary, octal and hexadecimal numbers, number base conversion.	1.2, 1.3	
	M 12/6			Introduction, Binary Numbers
3	T 13/6	Binary Codes, Binary Arithmetic.	1.3, 1.4, Handout	
4	W 14/6	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra. (HW#1 Distributed)	2.1, 2.2	
5	TH 15/6	Boolean functions, Algebraic manipulation, Complement of a function.	2.2	
6	S 17/6	Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums. (HW#1 Collected)	2.3	
	S 17/6			Basic Logic Functions
7	U 18/6	Map method of simplification: Two-, Three-, and Four-variable K-Map. (Quiz#1) (HW#2 Distributed)	2.4	
8	M 19/6	Map manipulation: Essential prime implicants, Nonessential prime implicants, Don't care conditions.	2.4	
	M 19/6			Hardware Implement. of Boolean Functions
9	T 20/6	Product-of-Sums Simplification, Five- and Six-variable K-map.	2.4, handout	
10	W 21/6	Nand and NOR gates: 2-level implementation. (HW#2 Collected)	2.6	
11	S 24/6	Nand and NOR gates: Multi-level implementation. (Quiz#2) (HW#3 Distributed)	2.6	
	S 24/6			Simplification

				of Boolean Functions
12	U 25/6	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Parity generation and checking.	2.7	
13	M 26/6	Combinational logic Design: Design Hierarchy, Top-Down Design, Analysis Procedure.	3.1, 3.2, 3.3	
	M 26/6			Design Procedure of Comb. Logic
14	T 27/6	Combinational logic Design: Design Procedure, Code Converters. (HW#3 Collected)	3.4	
15	W 28/6	Magnitude Comparator Design. (Exam I)	Handout	
16	S 1/7	Decoders and Encoders.	3.5, 3.6	
	S 1/7			Comparator Design
17	U 2/7	Multiplexers and Demultiplexers.	3.7	
18	M 3/7	Binary Adders: Ripple Carry Adder, Carry Look-Ahead Adder. (HW#4 Distributed)	3.8	
	M 3/7			Multiplier Design
19	T 4/7	Binary Subtraction, Binary Adders/Subtractors.	3.9, 3.10	
20	W 5/7	BCD Adder, Binary Multiplier.	3.11, 3.12	
21	S 8/7	Sequential Circuits: Latches, SR and D-latch, Clocked latch. (HW#4 Collected)	4.1, 4.2	
	S 8/7			Design Using MUXs
22	U 9/7	Flip-Flops: Master-Slave, Edge-Triggered. (Quiz#3) (HW#5 Distributed)	4.3	
23	M 10/7	Flip-Flops Characteristic Tables: D-FF, SR-FF, JK-FF, T-FF. (HW#5 Distributed)	4.3	
	M 10/7			Adder/Subtractor
24	T 11/7	Sequential Circuit Analysis: Input equations, State Table.	4.4	
25	W 12/7	Analysis with JK FFs, State Diagram. (HW#5 Collected)	4.4	
26	S 15/7	Sequential Circuit Design: Design procedure, Construction of state diagrams and state tables. (Exam II)	4.5	
27	U 16/7	Designing with D-FFs.	4.6	
28	M 17/7	Designing with JK-FFs, Flip-Flop Excitation Tables.	4.7	
	M 17/7			Design Using MSI Functions
29	T 18/7	State Reduction and State Assignment.	Handout	

30	W 19/7	Sequential Circuit Design Examples. (HW#6 Distributed)	Handout	
31	S 22/7	Registers, Shift Registers.	5.2, 5.3	
	S 22/7			Latches & FFs
32	U 23/7	Ripple Counter, Synchronous Binary Counters.	5.4, 5.5	
33	M 24/7	Design of Binary counter, Serial and Parallel Counters, Up-Down Binary Counter. (HW#6 Collected)	5.5	
	M 24/7			Design of Sequential Circuits
34	T 25/7	<i>Memory and Programmable Logic Devices:</i> Read-Only Memory. (Quiz#4)	6.1, 6.7	
35	W 26/7	Combinational Circuit Implementation with ROM.	6.7	
36	S 29/7	Programmable logic Array.	6.8	
	S 29/7			Design of Counters
37	U 30/7	Programmable Array logic.	6.9	
38	M 31/7	Review for final exam.		