

Magnitude Comparator

In this lesson you will learn about

1. Magnitude comparator
2. How to design a 4-bit comparator

Definition

A magnitude comparator is a combinational circuit that compares two numbers **A** & **B** to determine whether:

- $A > B$, or
- $A = B$, or
- $A < B$

Inputs

First n -bit number **A**

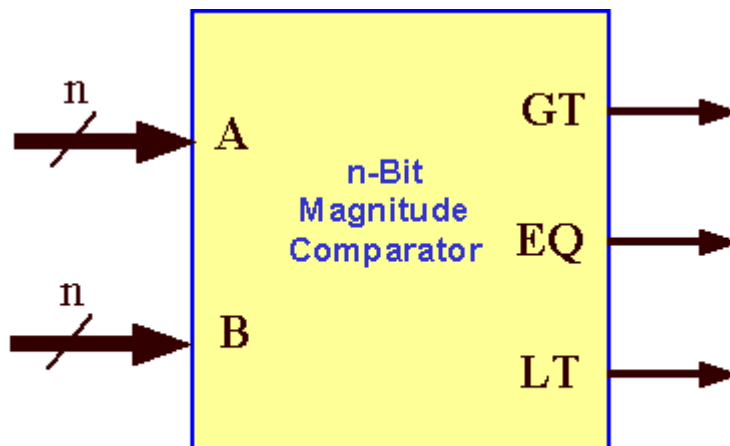
Second n -bit number **B**

Outputs

3 output signals (GT, EQ, LT), where:

1. $GT = 1$ IFF $A > B$
2. $EQ = 1$ IFF $A = B$
3. $LT = 1$ IFF $A < B$

Note: Exactly One of these 3 outputs equals 1, while the other 2 outputs are 0`s

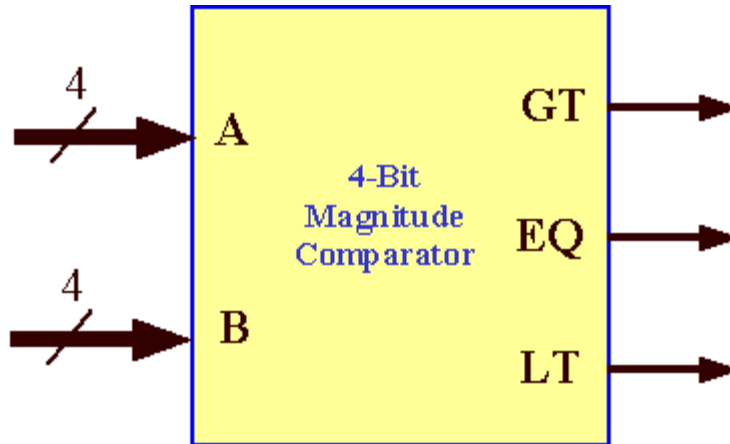


4-bit magnitude comparator

Inputs: 8-bits ($A \Rightarrow 4$ -bits, $B \Rightarrow 4$ -bits)

A and B are two 4-bit numbers

- Let $A = A_3A_2A_1A_0$, and
- Let $B = B_3B_2B_1B_0$
- Inputs have 2^8 (256) possible combinations
- Not easy to design using conventional techniques



The circuit possesses certain amount of regularity \Rightarrow *can be designed algorithmically*.

Design of the EQ output ($A = B$) in 4-bit magnitude comparator

Define $X_i = (A_i B_i) + (A_i' B_i')$

Thus $X_i = 1$ IFF $A_i = B_i \quad \forall i = 0, 1, 2 \text{ and } 3$

$X_i = 0$ IFF $A_i \neq B_i$

Condition for $A = B$

$EQ = 1$ (i.e., $A = B$) IFF

1. $A_3 = B_3 \rightarrow (X_3 = 1)$, and
2. $A_2 = B_2 \rightarrow (X_2 = 1)$, and
3. $A_1 = B_1 \rightarrow (X_1 = 1)$, and
4. $A_0 = B_0 \rightarrow (X_0 = 1)$.

Thus, $EQ = 1$ IFF $X_3 X_2 X_1 X_0 = 1$. In other words, $EQ = X_3 X_2 X_1 X_0$

Design of the GT output ($A > B$) 4-bit magnitude comparator

If $A_3 > B_3$, then $A > B$ ($GT = 1$) irrespective of the relative values of the other bits of A & B . Consider, for example, $A = 1000$ and $B = 0111$ where $A > B$.

This can be stated as $GT = 1$ if $A_3 B_3' = 1$

If $A_3 = B_3$ ($X_3 = 1$), we compare the next significant pair of bits (A_2 & B_2).

If $A_2 > B_2$ then $A > B$ ($GT = 1$) irrespective of the relative values of the other bits of A & B . Consider, for example, $A = 0100$ and $B = 0011$ where $A > B$.

This can be stated as $GT = 1$ if $X_3 A_2 B_2' = 1$

If $A_3 = B_3$ ($X_3 = 1$) and $A_2 = B_2$ ($X_2 = 1$), we compare the next significant pair of bits (A_1 & B_1).

If $A_1 > B_1$ then $A > B$ ($GT=1$) irrespective of the relative values of the remaining bits A_0 & B_0 . Consider, for example, $A = 0010$ and $B = 0001$ where $A > B$
 This can be stated as $GT=1$ if $\overline{X_3} \overline{X_2} A_1 B_1' = 1$

If $A_3 = B_3$ ($X_3 = 1$) and $A_2 = B_2$ ($X_2 = 1$) and $A_1 = B_1$ ($X_1 = 1$), we compare the next pair of bits (A_0 & B_0).

If $A_0 > B_0$ then $A > B$ ($GT=1$). This can be stated as $GT=1$ if $X_3 X_2 X_1 A_0 B_0' = 1$

To summarize, $GT = 1$ ($A > B$) IFF:

1. $A_3 B_3' = 1$, or
2. $\overline{X_3} A_2 B_2' = 1$, or
3. $\overline{X_3} \overline{X_2} A_1 B_1' = 1$, or
4. $\overline{X_3} \overline{X_2} \overline{X_1} A_0 B_0' = 1$

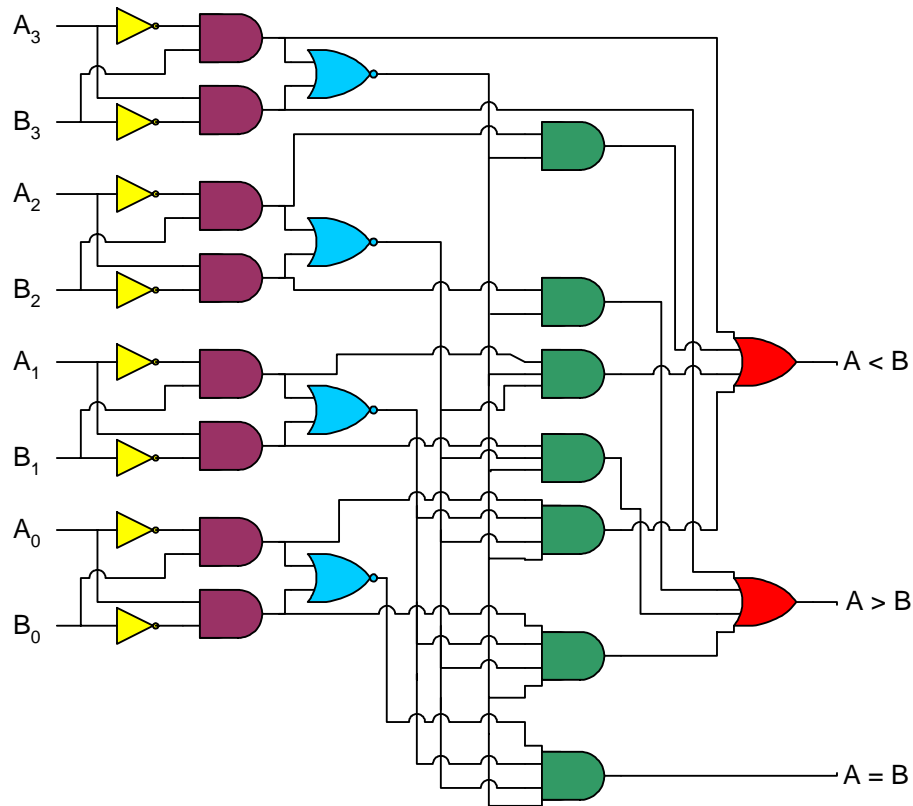
In other words, $GT = A_3 B_3' + \overline{X_3} A_2 B_2' + \overline{X_3} \overline{X_2} A_1 B_1' + \overline{X_3} \overline{X_2} \overline{X_1} A_0 B_0'$

Design of the LT output ($A < B$) 4-bit magnitude comparator

In the same manner as above, we can derive the expression of the LT ($A < B$) output

$$LT = B_3 A_3' + \overline{X_3} B_2 A_2' + \overline{X_3} \overline{X_2} B_1 A_1' + \overline{X_3} \overline{X_2} \overline{X_1} B_0 A_0'$$

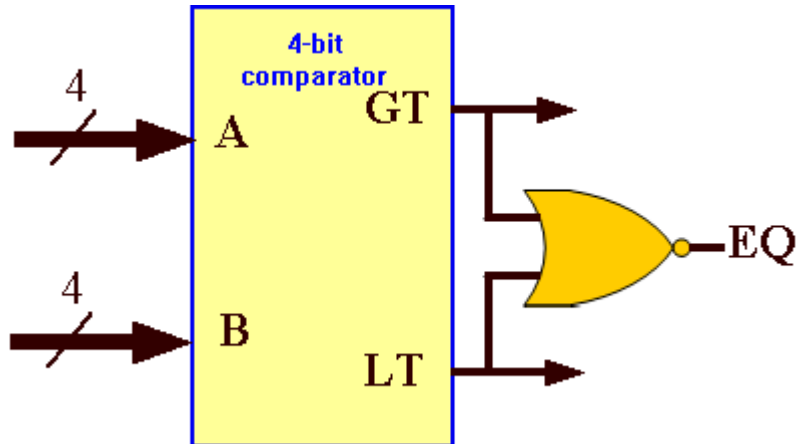
The gate implementation of the three output variables (EQ, GT & LT) is shown in the figure below.



Modification to the Design

The hardware in the comparator can be reduced by implementing only two outputs, and the third output can be obtained using these two outputs.

For example, if we have the LT and GT outputs, then the EQ output can be obtained by using only a NOR gate, as shown in the figure below.



Thus, when both the GT and LT outputs are zeros, then the 3rd one (i.e. EQ) is a '1'