KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 202 Digital Logic Design
Syllabus - Term 162

Catalog Description

Introduction to information representation and number systems. Boolean algebra and switching theory. Manipulation and minimization of completely and incompletely specified Boolean functions. Propagation delay, timing diagrams. Combinational circuits design using multiplexers, decoders, comparators and adders. Sequential circuit analysis and design, basic flip-flops, clocking and timing diagrams. Registers, counters, ROMs, PALs, PLAs and FPGA's. Introduction to Verilog.

Prerequisite: PHYS 102

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Office Hours ***UTR 12:15-1:00 PM, MW 11:00AM – 12:00PM and by appointment***

Course Learning Outcomes

1. Ability to use math and Boolean algebra in performing computations in various number systems and simplification of Boolean algebraic expressions.
2. Ability to design efficient combinational and sequential logic circuit implementations from functional description of digital systems.
3. Ability to use CAD tools to simulate and verify logic circuits.

Textbook

Alan B. Marcovitz , *Introduction to Logic Design*, Third Edition, McGraw-Hill, 2010.

Grading Policy

Discussions	5%	
Assignments	10%	
Quizzes	10%	
Exam I	20%	**(Sat., March 11, 1:00 PM)**
Exam II	25%	**(Sat., April 29, 1:00 PM)**
Final	30%	

- Attendance will be taken regularly. For each missed 3 classes, a penalty of 0.5 will be deducted.
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted but you will be penalized 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 10%.
- No makeup will be made for missing Quizzes or Exams.

Course Topics

Week	Topic
1	• Introduction. • Weighted Number Systems. Decimal, Binary, Octal and Hexadecimal. • Number base conversion (Dec to Bin, Oct, and Hex).
2	• Arithmetic in Binary and Hex (addition, subtraction& Multiplication) • BCD Codes: Excess-3 & other BCD codes, Character Storage, ASCII Code. Error Detection, Parity Bit. • Binary logic and gates, Truth tables, Boolean Algebra, Basic identities. Principle of duality, DeMorgan's Theorem. • Algebraic Manipulation of Boolean expressions.
3	• Algebraic Manipulation of Boolean expressions. • Canonical and Standard forms, Minterms, Maxterms, Sum of products & Products of Sums. • 2-Level gate implementation (SOP, POS). • From Truth tables to Boolean Expressions.
4	• Propagation delay. Timing diagrams. • Introduction to Verilog: Verilog Syntax, Definition of a Module, Gate Level Modeling, Using Modelsim simulation tool. Module Instantiation, Propagation Delay, Behavioral Modeling, Boolean Equation-Based Behavioral Models of Combinational Logic, Assign Statement, Propagation Delay & Continuous Assignment, Test Bench Example.
5-6	• Map method of simplification: 2, 3 and 4-variable maps. Implicants, Prime Implicants, Essential Prime Implicants. • POS simplification. • Don't care conditions and simplification. • Universal gates (NAND, NOR) • Implementation using Nand and NOR gates: 2-level & Multilevel implementation. • Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.
7-8	• Combinational Circuit Design Procedure & Examples. • Iterative combinational circuit design • Half and Full Adders. • Ripple Carry Adder design and ***Delay*** analysis of RCA • Signed Numbers: sign-magnitude, 1`s complement, and 2`s complement. • Signed Binary Arithmetic. (Addition and Subtraction). • Binary Adder-Subtractor.
9-10	• Decoders 2x4, 3x8, 4x16. Designing large decoders from smaller decoders. Function implementation using decoders. • Encoders: Priority Encoders. • Multiplexers**:** 2x1, 4x1. Constructing large MUXs from smaller ones. • Function implementation using multiplexers. • MSI Design Examples
11-13	• Introduction to Verilog: Verilog Operators, Behavioral Description of an Adder, Always block, Procedural Assignment, If Statements, Case Statements, Comparator, Arithmetic & Logic Unit. Multiplexor, Encoder, Priority Encoder, Decoder, Seven Segment Display Decoder.

	• Sequential Circuits: Latches, Clocked latches: SR, D. Flip-Flops: Master-Slave, D-FF. • Analysis of Sequential Circuits. State table, State diagram. • Mealy vs. Moore machine. • Sequential Circuit Design. Design procedure, State diagrams and state tables. • Asynchronous/Direct Clear and Set Inputs. Setup, Hold, FF propagation delay. Calculation of maximum clock frequency.
14-15	• Verilog modeling of D-Latch, D Flip Flop – Synchronous Set/Reset, D Flip Flop–Asynchronous Set/Reset. Verilog Structural modeling of sequential circuits, Verilog FSM modeling. • Registers, Registers with parallel load. • Shift Registers. Bi-directional shift register. Applications of shift registers • Synchronous Binary Counters*:* Up-Down Counters • Counters with Parallel load, enable, synchronous clear and asynchronous clear. • Use of available counters to build counters of different count. • Verilog modeling of: Parallel Load Register, Shift Register, Up-Down Counter.. • Combinational & Sequential Circuit Implementation with ROM. • Sequential Circuit Implementation using ROMs.