KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 202 Digital Logic Design
Syllabus - Term 092

Catalog Description

Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuit analysis and design, multiplexers, decoders, adders. Sequential circuit analysis and design, basic flip-flops, clocking, and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations. Machine-level programming.

Prerequisite: PHYS 102

Instructor Dr. Aiman H. El-Maleh. Room: 22/318 Phone: 2811
Email: aimane@ccse.kfupm.edu.sa

Office Hours UT 10:00-11:00**,** and by appointment

Course Learning Outcomes

1. Ability to use math and Boolean algebra in performing computations in various number systems and simplification of Boolean algebraic expressions.
2. Ability to design efficient combinational and sequential logic circuit implementations from functional description of digital systems.
3. Ability to use CAD tools to simulate and verify logic circuits.

Course Material

1. **Textbook** Morris Mano and Charles Kime, *Logic and Computer Design Fundamentals*, Third Edition, Prentice Hall International, 2004.
2. **Course CD** A CD containing all course lectures with animations and sound is available. The material can be downloaded from ftp://rahma.ccse.kfupm.edu.sa/export/tools/material/On%20Line%20Course%20Material/. The material is divided into 6 units with several lessons in each unit.

Grading Policy

Discussions & Reflections	5%	
Assignments	10%	
Quizzes	10%	
Exam I	20%	(Thur. March 25, 2010)
Exam II	25%	(Thur. May 13, 2010)
Final	30%	

- Attendance will be taken regularly,

- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- No makeup will be made for missing Quizzes or Exams.

Course Topics

Week	Topic	CD Material	
		Unit	Lessons
1	Introduction, Number System and Arithmetic	I	1, 2 & 3
2	Number Base Conversion, Signed Numbers and Signed Numbers Arithmetic	I	4, 5 & 6
3	Codes and Binary Logic, Basic Identities, Algebraic Simplification	I II	7 1
4	Canonical and Standard Forms, Physical Properties of Gates	II	2 & 3
5	Logic Simplification using K-Maps, K-Maps Manipulation	II	4 & 5
6	2-Level and Multi-Level implementations, Universal Gates	II	6 & 7
7	Combinational Logic and Adders	III	1 & 2
8	Carry-Look-Ahead Adders and MSI Parts	III	3 & 4
9	Design with MSI Parts	III	5, 6 & 7
10	Sequential Circuits, Latches and FFs	IV	1 & 2
11	Design of Sequential Circuits	IV	3 & 4
12	Analysis of Sequential Circuits	IV	5
13	Registers and Counters	V	1 – 4
14	Programmable Logic	VI	1 & 2

Online Lessons included on the course CD

Unit I	
Number System and Codes	
1	Introduction. Information Processing, and representation. Digital vs Analog quantities.
2	Number Systems. Binary, Octal and Hexadecimal #'s
3	Number System Arithmetic. Binary arith (Addition, Subtraction & Multiplication). Arith in other systems.
4	Number base conversion (Dec to Bin, Oct, and Hex, General). Conv (Bin, OCT, Hex)
5	Binary Storage & Registers. Signed Binary Number representation, Signed Mag, R's &(R-1)'s Complement
6	Signed Binary Addition and Subtraction. R's Complement. Signed Binary Addition and Subtraction. (R-1)'s Complement
7	Codes. BCD, Excess-3, Parity Bits, ASCII & Uni-Codes
Unit II	
Binary Logic & Gates	
1	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra. Algebraic manipulation, Complement of a function.
2	Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums.
3	Physical properties of gates: fan-in, fan-out, propagation delay. Timing diagrams. Tri-state drivers.
4	***Map method of simplification***: Two-, Three-, and Four-variable K-Map.
5	***Map manipulation:*** Essential prime implicants, Non-essential prime implicants, Simplification procedure, POS simplification, Don't care conditions and simplification, Five, and Six-variable K-Map.
6	Universal gates; ***NAND, NOR gates:*** 2-level implementation. ***Multilevel Circuits***.
7	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.
Unit III	
Combinational Logic	
1	Combinational Logic, Design Procedure & Examples.
2	Half and Full Adders, Half and Full Subtractor

	Ripple Carry Adder design and ***delay*** analysis ***Binary Adders: 4-Bit* Ripple Carry Adder,**
3	**Carry Look-Ahead Adder, Binary Adder-Subtractor**. BCD Adder, Binary Multiplier
4	MSI parts. Decoders, Decoder expansion, combinational logic implementation using decoders, Encoders & Priority Encoders
5	Multiplexers, Function Implementation using multiplexers, Demultiplexers
6	Magnitude Comparator.
7	Examples of MSI designs
Unit IV	
Sequential Circuits	
1	***Sequential Circuits:*** Latches, Clocked latches: SR , D, T and JK. Race problem in clocked JK-Latch. ***Function & Excitation Tables of clocked latches:*** SR, D, and JK.
2	***Flip-Flops:*** Master-Slave, T-FF. Function & Excitation Tables of T-FF. ***Asynchronous/Direct Clear and Set Inputs.*** Setup, Hold
3	***Sequential Circuit Design***: Excitation Tables. Design procedure, State diagrams and state tables.
4	***Sequential Circuit Analysis:*** Input equations, State table.
5	Mealy vs. Moore models of FSMs. Examples.
Unit V	
Registers & Counters	
1	Registers, Registers with parallel load, Shift Registers. Bi-directional shift register.
2	Synchronous Binary Counters*:* Up-Down Counters.
3	Counters with Parallel load, enable, synchronous clear and asynchronous clear. Use of available counters to build counters of different count.
4	Other counters: *Ripple Counter*, Arbitrary Count Sequence.
Unit VI	
Memory & PLDs	
1	Memory devices: RAMs & ROMs . Combinational Circuit Implementation with ROM
2	Programmable Logic Devices: PLAs, PALs, FPGA'a