KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 200 Fundamentals of Computer Engineering
Syllabus - Term 041

Catalog Description

Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuits analysis and design, multiplexers, decoders and adders. Sequential circuit analysis and design, basic flip-flops, clocking and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations. ***(Prerequisite: PHYS 102)***

Instructor

Aiman El-Maleh **Room** 22-318 **Phone**: 2811 **e-mail**:aimane@ccse

Class

Time 9:00 - 9:50 SMW **Location** **Room** 24-120

Course Delivery:

This course will be delivered in a semi-online manner. A *CD* containing all course lectures with animations and sound will be given to each student. Students are expected to study, on their own, these lessons/lectures. The course instructor will deliver a lecture each Saturday to guide students and respond to their questions. In addition, a problem-solving tutorial session will be held every Wednesday. Quizzes will be conducted on Mondays every 2 weeks.

Course Material:

1. **Online Lessons CD**
   The CD contains all course lectures with animations and sound. The material is divided into 6 units with several lessons in each unit.
2. **Text Book:** Morris Mano and Charles Kime, *Logic and Computer Design Fundamentals*, Second Edition, Prentice Hall International, 2000.

Grading Policy:

Laboratory	20%
Quizzes	15%
Exam I	15% (*5:30pm Monday, October 11*)
Exam II	20% (*5:15pm Monday, December 6*)
Final	30%

Course Road Map & Weekly Breakdown

Week	CD Self-Study Material		Saturday Lecture	Wednesday Tutorial	Mon day	Book Ref.
	Unit	Lessons				
1	1	1,2 and 3	General introduction & course guidelines	Lecture (Num Sys Arith)		1.1-1.3
2	1	4, 5 and 6	Base conversion	Numb Sys & Conversion		3.9-3.10
3	1 2	Lesson 7. Lesson 1.	Signed Numbers Arithmetic	Signed Number Arith		1.4 -1.5 & 2.1-2.2
4	2	2 & 3	Boolean Algebraic, Manipulation	Boolean Algebra	Quiz 1	2.3&2.8
5	2	4 & 5	Standard & Canonical forms & introduce K-Maps	U2L 2&3		2.4-2.5
6	2	6 & 7	***K-Map examples***	K-Maps	Quiz 2	2.6-2.7

7	3	1 & 2	***CL Design Procedure***	2-Level SOP, POS, AOI, OAI, XOR		3.1-3.4 & 3.8
8	3	3 & 4	Ripple Carry Adder & Delay	U3 L 1 & 2	Quiz 3	3.9-3.11 & 3.5-3.6
9	3	5, 6, 7	MSI parts	RCA & CLA		3.7
10	4	1 & 2	Introd. Seq Systems	MSI	Quiz 4	4.1-4.3
11	4	3 & 4	Edge Trig. FFs & Excit Tables	Latches & FFs		4.4 -4.7
12	4	5	Seq Design (overall)	Seq. Design & Analysis	Quiz 5	4.4-4.7
13	5	1-4	***Registers & Counters***	Moore & Mealy		5.1-5.6
14	6	1 & 2	***Memories & PLDs***	Registers & Counters	Quiz 6	6.1-6.2 & 6.5-6.9
15			***Wrap-up***	Memories & PLDs		

Online Lessons included on the course CD

Unit I	
Number System and Codes	
1	Introduction. Information Processing, and representation. Digital vs Analog quantities.
2	Number Systems. Binary, Octal and Hexadecimal #'s
3	Number System Arithmetic. Binary arith (Addition, Subtraction & Multiplication). Arith in other systems.
4	Number base conversion (Dec to Bin, Oct, and Hex, General). Conv (Bin, OCT, Hex)
5	Binary Storage & Registers. Signed Binary Number representation, Signed Mag, R's &(R-1)'s Complement
6	Signed Binary Addition and Subtraction. R's Complement. Signed Binary Addition and Subtraction. (R-1)'s Complement
7	Codes. BCD, Excess-3, Parity Bits, ASCII & Uni-Codes
Unit II	
Binary Logic & Gates	
1	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra. Algebraic manipulation, Complement of a function.
2	Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums.
3	Physical properties of gates: fan-in, fan-out, propagation delay. Timing diagrams. Tri-state drivers.
4	***Map method of simplification***: Two-, Three-, and Four-variable K-Map.
5	***Map manipulation:*** Essential prime implicants, Non-essential prime implicants, Simplification procedure, POS simplification, Don't care conditions and simplification, Five, and Six-variable K-Map.
6	Universal gates; ***NAND, NOR gates:*** 2-level implementation. ***Multilevel Circuits***.
7	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.
Unit III	
Combinational Logic	
1	Combinational Logic, Design Procedure & Examples.
2	Half and Full Adders, Half and Full Subtractor Ripple Carry Adder design and ***delay*** analysis ***Binary Adders: 4-Bit* Ripple Carry Adder,**
3	**Carry Look-Ahead Adder, Binary Adder-Subtractor**. BCD Adder, Binary Multiplier
4	MSI parts. Decoders, Decoder expansion, combinational logic implementation using decoders, Encoders & Priority Encoders
5	Multiplexers, Function Implementation using multiplexers, Demultiplexers
6	Magnitude Comparator.
7	Examples of MSI designs
Unit IV	
Sequential Circuits	
1	***Sequential Circuits:*** Latches, Clocked latches: SR , D, T and JK. Race problem in clocked JK-Latch. ***Function & Excitation Tables of clocked latches:*** SR, D, and JK.
2	***Flip-Flops:*** Master-Slave, T-FF. Function & Excitation Tables of T-FF. ***Asynchronous/Direct Clear and Set Inputs.*** Setup, Hold
3	***Sequential Circuit Design***: Excitation Tables. Design procedure, State diagrams and state tables.
4	***Sequential Circuit Analysis:*** Input equations, State table.

5	Mealy vs. Moore models of FSMs. Examples.
Unit V	
Registers & Counters	
1	Registers, Registers with parallel load, Shift Registers. Bi-directional shift register.
2	Synchronous Binary Counters*:* Up-Down Counters.
3	Counters with Parallel load, enable, synchronous clear and asynchronous clear. Use of available counters to build counters of different count.
4	Other counters: *Ripple Counter*, Arbitrary Count Sequence.
Unit VI	
Memory & PLDs	
1	Memory devices: RAMs & ROMs . Combinational Circuit Implementation with ROM
2	Programmable Logic Devices: PLAs, PALs, FPGA'a