COE 200
Fundamentals of Computer Engineering
Syllabus – Term 051

Catalog Description
Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuits analysis and design, multiplexers, decoders and adders. Sequential circuit analysis and design, basic flip-flops, clocking and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations. (Prerequisite: PHYS 102)

Instructor
Dr. Abdelhafid Bouhraoua
Office: Building 22, Room 137-1
Phone: 2178
Fax: 3059
Email: abouh@ccse.kfupm.edu.sa
URL: http://www.ccse.kfupm.edu.sa/~abouh

Course Material
2. Course CD: A CD containing all course lectures with animations and sound is available. The material can be downloaded from the web page.

Grading Policy

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Laboratory</td>
<td>20%</td>
</tr>
<tr>
<td>Assignments and Quizzes</td>
<td>15%</td>
</tr>
<tr>
<td>Exam I &amp; Exam II</td>
<td>35%</td>
</tr>
<tr>
<td>Final</td>
<td>30%</td>
</tr>
</tbody>
</table>

- Assignments include written and programming assignments
- Lowest two marks of the quizzes and assignments dropped
- Lowest exam counted as 15% and highest exam counted as 20%
# Course Road Map & Weekly Breakdown

<table>
<thead>
<tr>
<th>Week</th>
<th>Topic</th>
<th>CD Material</th>
<th>Book Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><strong>Introduction, Number System and Arithmetic</strong></td>
<td>1, 2 &amp; 3</td>
<td>1.1-1.3</td>
</tr>
<tr>
<td>2</td>
<td><strong>Number Base conversion, Signed Numbers and Signed Numbers Arithmetic</strong></td>
<td>4, 5 &amp; 6</td>
<td>3.9-3.10</td>
</tr>
<tr>
<td>3</td>
<td><strong>Codes and Binary Logic, Basic Identities, Algebraic Simplification</strong></td>
<td>Lesson 7 Lesson 1</td>
<td>1.4 -1.5 &amp; 2.1-2.2</td>
</tr>
<tr>
<td>4</td>
<td><strong>Canonical and Standard Forms, Physical Properties of Gates</strong></td>
<td>2 &amp; 3</td>
<td>2.3&amp;2.8</td>
</tr>
<tr>
<td>5</td>
<td><strong>Logic Simplification using K-Maps, K-Maps manipulation</strong></td>
<td>4 &amp; 5</td>
<td>2.4-2.5</td>
</tr>
<tr>
<td>6</td>
<td><strong>2-Level and Multi-level implementations, Universal Gates</strong></td>
<td>6 &amp; 7</td>
<td>2.6-2.7</td>
</tr>
<tr>
<td>7</td>
<td><strong>Combinational Logic and Adders</strong></td>
<td>1 &amp; 2</td>
<td>3.1-3.4 &amp; 3.8</td>
</tr>
<tr>
<td>8</td>
<td><strong>Carry-Look-Ahead Adders and MSI Parts</strong></td>
<td>3 &amp; 4</td>
<td>3.9-3.11 &amp; 3.5-3.6</td>
</tr>
<tr>
<td>9</td>
<td><strong>Design with MSI Parts</strong></td>
<td>5, 6 &amp; 7</td>
<td>3.7</td>
</tr>
<tr>
<td>10</td>
<td><strong>Sequential Circuits, Latches and FFs</strong></td>
<td>1 &amp; 2</td>
<td>4.1-4.3</td>
</tr>
<tr>
<td>11</td>
<td><strong>Design of Sequential Circuits</strong></td>
<td>3 &amp; 4</td>
<td>4.4 -4.7</td>
</tr>
<tr>
<td>12</td>
<td><strong>Analysis of Sequential Circuits</strong></td>
<td>5</td>
<td>4.4-4.7</td>
</tr>
<tr>
<td>13</td>
<td><strong>Registers and Counters</strong></td>
<td>1 - 4</td>
<td>5.1-5.6</td>
</tr>
<tr>
<td>14</td>
<td><strong>Programmable Logic</strong></td>
<td>1 &amp; 2</td>
<td>6.1-6.2 &amp; 6.5-6.9</td>
</tr>
</tbody>
</table>

### Online Lessons included on the course CD

#### Unit I: Number System and Codes

2. Number Systems. Binary, Octal and Hexadecimal #'s
4. Number base conversion (Dec to Bin, Oct, and Hex, General). Conv (Bin, OCT, Hex)
5. Binary Storage & Registers. Signed Binary Number representation, Signed Mag, R’s & (R-1)’s Complement
7. Codes. BCD, Excess-3, Parity Bits, ASCII & Uni-Codes

#### Unit II: Binary Logic & Gates

2. Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums.
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Universal gates; NAND, NOR gates: 2-level implementation. Multilevel Circuits.</td>
</tr>
<tr>
<td>7</td>
<td>Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.</td>
</tr>
</tbody>
</table>

Unit III: Combinational Logic

<table>
<thead>
<tr>
<th></th>
<th>Combinational Logic, Design Procedure &amp; Examples.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Half and Full Adders, Half and Full Subtractor</td>
</tr>
<tr>
<td></td>
<td>Ripple Carry Adder design and delay analysis</td>
</tr>
<tr>
<td></td>
<td>Binary Adders: 4-Bit Ripple Carry Adder,</td>
</tr>
<tr>
<td>3</td>
<td>Carry Look-Ahead Adder, Binary Adder-Subtractor. BCD Adder, Binary Multiplier</td>
</tr>
<tr>
<td>4</td>
<td>MSI parts. Decoders, Decoder expansion, combinational logic implementation using decoders, Encoders &amp; Priority Encoders</td>
</tr>
<tr>
<td>5</td>
<td>Multiplexers, Function Implementation using multiplexers, Demultiplexers</td>
</tr>
<tr>
<td>6</td>
<td>Magnitude Comparator.</td>
</tr>
<tr>
<td>7</td>
<td>Examples of MSI designs</td>
</tr>
</tbody>
</table>

Unit IV: Sequential Circuits

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Flip-Flops: Master-Slave, T-FF. Function &amp; Excitation Tables of T-FF. Asynchronous/Direct Clear and Set Inputs. Setup, Hold</td>
</tr>
<tr>
<td>3</td>
<td>Sequential Circuit Design: Excitation Tables. Design procedure, State diagrams and state tables.</td>
</tr>
<tr>
<td>4</td>
<td>Sequential Circuit Analysis: Input equations, State table.</td>
</tr>
<tr>
<td>5</td>
<td>Mealy vs. Moore models of FSMs. Examples.</td>
</tr>
</tbody>
</table>

Unit V: Registers & Counters

<table>
<thead>
<tr>
<th></th>
<th>Registers, Registers with parallel load, Shift Registers. Bi-directional shift register.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Synchronous Binary Counters: Up-Down Counters.</td>
</tr>
<tr>
<td>3</td>
<td>Counters with Parallel load, enable, synchronous clear and asynchronous clear. Use of available counters to build counters of different count.</td>
</tr>
<tr>
<td>4</td>
<td>Other counters: Ripple Counter, Arbitrary Count Sequence.</td>
</tr>
</tbody>
</table>

Unit VI: Memory & PLDs

|   | Memory devices: RAMs & ROMs. Combinational Circuit Implementation with ROM |
Ethics Policy

- All assignments are individual and only individual work will be accepted. Detected copies of assignments (written or programming assignments) will result in zeros for the whole group (including the student who actually solved the problem).

- Using unauthorized information or notes on an examination, peeking at others work, or altering a graded exam to claim more grades are severe violations of academic honesty. Remember that if you cheat, you are cheating no one but yourself. Detected situations will result in failing grades in the course, and depending on the severity of the situation, some cases may possibly end up in suspension from the university.