KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS
COLLEGE OF COMPUTER SCIENCE AND ENGINEERING
COMPUTER ENGINEERING DEPARTMENT

COE 205
Computer Organization & Assembly Language
Syllabus – Term 061

Catalog Description

Introduction to computer organization – Signed and unsigned number representation – Character representation – ASCII codes – Assembly language programming: instruction format and type, memory and I/O instructions, dataflow, arithmetic and logic instructions, flow control instructions, addressing modes, stack operations and interrupts – Datapath and control unit organization – RTL, microprogramming and hardwired control – Practice of assembly language programming.

Prerequisite: COE 200 and ICS 201

Instructor   **Dr. Abdelhafid Bouhraoua** Room: 22/137-1   Phone: 2178
                        Email: abouh@ccse.kfupm.edu.sa

Office Hours   SMW 9:00 AM – 11:00 AM (and by appointment)

Course Objectives

1. Comprehend computer organization and how a computer system works
2. Proficiency in assembly language programming in general and for the 80x86 family in particular. Ability to program efficiently in assembly language by understanding the advantages and constraints of such an exercise. The student should be able to analyze, debug and test programs written in assembly language.
3. Knowledge of computer organization and CPU organization. CPU-Memory interaction. Input/Outputs and buses. Knowledge of CPU internal typical architecture. Datapath architecture and Control unit architecture.

Course Outcome

1. Knowledge of basic computer organization, information representation, and basic assembly language concepts.

2. Ability to analyze, design, implement, and test assembly language programs.

3. Ability to use tools and skills in analyzing and debugging assembly language programs.

4. Ability to design the datapath and control unit of a simple CPU.

5. Ability to demonstrate self-learning capability.

6. Ability to work in a team.

Textbook References

1. Kip Irvine, *Assembly Language for Intel-Based Computers*, Prentice Hall, 4th Edition, 2003, ISBN: 0130910139

2. Vincent P. Heuring & Harry F. Jordan, *Computer Systems Design and Architecture*, Addison Wesley, 1997. ISBN: 0-8053-4330-X.

3. Online Material: http://assembly.pc.ccse.kfupm.edu.sa

Grading Policy

Laboratory	20%
Quizzes and Assignments	25%
Major Exam 1 and Major Exam 2	35%
Final	20%

- Assignments include written and programming assignments
- Lowest two, three or four marks of the quizzes and assignments dropped
- Lowest exam counted as 15% and highest exam counted as 20%
- Assignments are to be submitted in class or by email in the specified due date.
- Late assignments will be accepted for five days after the due date and be penalized 10% per each late day

Exam Dates

Major Exam 1		Monday October 9th 2006	9:00-11:00 PM
	or	Saturday Nov. 4th 2006	7:00-9:00 PM
Major Exam 2		Wednesday December 13th 2006	7:00-9:00 PM
Final Exam		Saturday January 20th 2007	7:30-9:30 AM

Course Topics

1. **Introduction and Computer Organization** – *2 weeks*
   Computer Organization: How a computer is organized. What is an instruction. Instruction fetch/execute cycle. Computer components. Data Representation.

2. **Assembly Language Concepts – *2 weeks***
   Assembly language vs. high-level language. Assembly language format. Directives .vs. instructions. Constants and variables. Addressing modes

3. **Pentium Assembly Langugae Programming – *6 ⅓ weeks***
   Register Set. MOV instructions. Arithmetic instructions and flags (ADD, ADC, SUB, SBB, INC, DEC, MUL, IMUL, DIV, IDIV). Compare, Sequence control (CMP, JMP, Conditional jumps, LOOP). Logic instructions, shift and rotate.

Stack operations. Subroutines. Macros. I/Os (IN, OUT). String manipulation instructions. Interrupt and interrupt processing (INT, RET).

4. **CPU Design – *4 weeks***
   CPU design fundamental parameters and consequences. Register transfer. Datapath typical organization: 1-bus, 2-bus and 3-bus. Fetch and execute phases of instruction processing. Performance issues. Memory interfacing. Control unit organization. Hardwired control unit design. Microprogramming. Horizontal and Vertical microprogramming. Microprogrammed control unit design.

5. **Instruction Format Design Issues - *1⅔ weeks***
   Goals and practices in designing instruction formats. Fixed vs. variable formats. Format lengths. Number of arguments.

Ethics Policy

- All assignments are individual and only individual work will be accepted. Detected copies of assignments (written or programming assignments) will result in zeros for the whole group (including the student who actually solved the problem)
- Using unauthorized information or notes on an examination, peeking at others work, or altering a graded exam to claim more grades are severe violations of academic honesty. Remember that if you cheat, you are cheating no one but yourself. Detected situations will result in failing grades in the course, and depending on the severity of the situation, some cases may possibly end up in suspension from the university.